Trigger Tasks   3 May 2001

Introduction

The Technical Review (6/12/2000) of the BTEV trigger, which provided support material for the Fermilab PAC, identified some high-risk issues in our design.

- o Lack of adequate queuing simulations and timing studies.
- o Assembly language code has not been run on a DSP or on a DSP simulator.
- o Data integrity robustness, control, and monitoring need to be addressed.

These issues need to be addressed in preparation for the BTEV TDR.

Overview

- o Review hardware of the baseline design for Level 1 (block diagram)
- o Describe functions performed by each piece of the hardware
- o Identify asks to be completed by February 2, 2002

Pixel Data Combiner (Sergio Zimmermann & Gustavo Cancelo)

Functions performed by the pixel readout:
- Receives data from FPIX chips.
- Adds additional time-stamp bits.
- Distributes data to fiber links and equalizes data flow rates.
- Imposes pixel-hit limits on beam crossings with too much data (warning flag).

Tasks for Feb 2002:
- Hardware design. (Pixel Group: Sergio)
- Data-flow simulation. (Trigger Group: Gustavo) Well Underway

Pixel Processor (Gustavo Cancelo, Ken Treptow, Greg Deuerling)

Functions performed by the pixel processor:

1) Time-stamp ordering.
- Receives data that is not ordered in time.
- Use time stamps to order and group data for each beam crossing.
- Large data buffer (delay buffer) with space allacated for each beam crossing.

2) Ll buffer management.
- Data is directed to an Ll buffer for the DAQ.
- Data is also directed to the input of the Level 1 trigger.

3) Cluster finding.
- Find pixel clusters using pixels in the same row (i.e. not across column boundaries).
- Tag clusters that exceed a maximum cluster size (other types of warning flags?).

4) Row:column to x:y translation using lookup table.
- Tag pixel clusters that fall in "seed" regions (inner and outer or phi regions).
- Duplicate pixel clusters that are close to boundary edges (is this necessary?).

Tasks for Feb 2002:
- Whole Subsystem data-flow simulation. (Gustavo)

1) Time-stamp ordering. (Ted, Ken)
- Possible VHDL code and simulation.
- No prototype.

2) Ll buffer management.
- We expect to get VHDL code and hardware architecture from the BTeV DAQ group.
- We would like to see the DAQ group produce a prototype.
- Data flow simulation.

3) Cluster finding.   (Ted, Ken)
- Possible VHDL code and simulation.
- Probably a prototype.

4) Row:column to x:y translation using lookup table. (Ted, Ken)
- VHDL code and simulation.
- Perhaps a prototype.

5) Pixel hit generator. (diagnostic tool)
- Design and build an FPGA that can generate a data stream from simulated data.
- OR, see if we can use one of the pattern generators used in the ESE department.

FPGA Tracker (Ted Zmuda, Ken Treptow, & Greg Deuerling)

Functions performed by the FPGA tracker:
    1) Seed-region selector. (This may be done by row:column to x:y translator)

- Identify pixel clusters in inner and outer seed regions.
- The size of the seed region is fixed each time the Level 1 trigger is initialized.

    2) Segment processor.

- Finds inner and outer track segments.
- Content-addressable memory implemented in FPGAs.

    3) Segment buffer.

- Buffers inner and outer track segments for DSP.

    4) Scheduler and Router.

- Selects DSP for track/vertex reconstruction.

Tasks for Feb 2002:

    1) Seed-region selector. (Should be done by a tag bit in the row:colmn to xy translator, above)

- VHDL code and simulation.
- Perhaps a prototype.

    2) Segment processor. <mark>Ted and Ken are working on this</mark>

- VHDL code and simulation.
- Build a prototype. (High priority)

    3) Segment buffer.   (DAQ VHDL)

- Probably a special L1 Buffer.

    4) Switch. (Bowden)

- ???? (Architecture dependent)

DSP Farm (Dave Berg, Erik Gottschalk & Greg Deuerling)

Functions performed by the DSP farm:
1) Track/vertex reconstruction.
2) Track/vertex cuts.
3) Trigger decision.

Tasks for Feb 2002:
- Real-time operating system and monitor. (Dave + Erik + DPBIOS)
- Application software. (Erik, Mike)
- Benchmark software for different DSPs on DSKs. (Erik, Mike)
- Prototype with new DSP Farm hardware. (Dave, Greg)
- Define link needed for messages as above.
- Specify hardware, computer, and link card.

Control & Monitoring (Dave Berg, Greg Deuerling, Vince Pavlicek)

Functions performed by the control & monitoring hardware:
1) Control.
2) Monitoring.
3) Initialization.

Tasks (some or all of these should be addressed by Feb, 2002):
What is the effect of the NSF ITR Grant here?
- Hardware definition for control & monitoring link: USB, ARCNET, host port.   (Greg)
- Define the protocol for the link. (Vince)

Global Level 1 (unknown … Mark?)

Functions performed by the control & monitoring hardware:
- Accept Trigger messages from the trigger subsystems
- Make trigger decision
- Pass decision on to DAQ

Tasks for Feb 2002:
- Define link needed for messages as above.
- Specify hardware, computer, and link card as above.

Conclusion

1) We have identified pixel-trigger tasks to be completed by February 2, 2002
- We have lots of tasks for the trigger group
- We would like the pixel group to finalize the design of the "pixel readout".
- We require hardware guidance from the DAQ group for the Level 1 buffer.

2) These tasks address issues raised by the Technical Review of the BTEV Trigger
- Queuing simulations and timing studies.
- Trigger code has not been run on a DSP or DSP simulator.

3) These tasks DO NOT DIRECTLY address control & monitoring, data integrity, robustness.
- Uncertain as to what is needed by February 2002
- We are certain that we can use help with this aspect of the pixel trigger